Abarajithan Gnaneswaran

{abapages.com} {github.com/abarajithan11} {linkedin.com/in/abarajithan11} {agnaneswaran@ucsd.edu}

EDUCATION

University of California, San Diego Sep 2022 - 2027 [anticipated]

- PhD student (Computer Engineering) advised by Prof. Ryan Kastner.

University of Moratuwa (Sri Lanka) Dec 2015 - Feb 2020

- BSc. (First Class Honors) in Electronics and Telecommunications Engineering; GPA: 3.86/4.0 (3.92/4.2)

EXPERIENCE

AMD (San Jose): Summer Intern, R&D Team Jun 2024 - Sep 2024

- Investigated runtime mechanisms for partially switching AMD AI Engine dataflow configurations; assessed feasibility, constraints, and expected performance implications.
- Built and ran benchmarking/profiling experiments to isolate bottlenecks across the HW/SW stack.

Qualcomm (San Diego): Interim Intern, GSoC Integration Team Jun 2023 - Sep 2023

- Designed a parameterized Generic Software Interface IP with a NoC bridge (parameterized multi-slave; serialized and unserialized modes), and built automation to generate and verify the IP with UVM VIPs.
- Conducted architectural feasibility analysis for migrating DL1 SoC IP from AHB to a proprietary serialized bus; compared latency/throughput tradeoffs across representative use cases.

Lemurian Labs (Canada - remote): RTL Design Engineer (R&D) Dec 2020 - Aug 2022

- As the first hire, designed & built the foundational compute core to accelerate AI with a novel arithmetic system.
- Collaborated across architecture, PD, and verification. Built CI/CD pipelines to verify compute engines.

CSIRO (Australia): R&D Intern at DATA61 Jul 2018 - Dec 2018

- Built a DNN training-to-edge pipeline on supercomputer→TensorRT→ROS/Jetson TX2 for DARPA SubT work.

PROJECTS

- **Hardware Fuzzing for AXI:** A standardized testbed to evaluate hardware fuzzers like Intel PreSiFuzz and RFuzz. Maps fuzzer bytestreams into AXI transactions and tests SoC IPs with automatically injected bugs.

- **CGRA4ML:** An open-source, automated framework for scientific edge computing. Maps DNNs from Python to custom, parameterizable SystemVerilog CGRAs with C firmware, targeting FPGAs and custom ASICs.

- **FireBridge:** A framework for system-level verification enabling rapid FW/HW co-development. Bridges SystemVerilog AXI subsystems to real C firmware via DPI-C, without simulating a CPU.

- **AXIS Systolic Array:** A lightweight, highly parameterizable systolic array in SV, integrated with Ibex-SoC via AXI DMAs, a custom DMA controller, and corresponding C firmware. Currently being formally verified.

- **SystemVerilog course for 300 students:** 64-hour course, conducted in collaboration with Synopsys, covering RTL design, randomized transactional testbenches, AXI protocol design, FPGA and ASIC flow labs.

PUBLICATIONS

- **CGRA4ML**: A Hardware/Software Framework to Implement Neural Networks for Scientific Edge Computing, ACM Transactions on Reconfigurable Technology and Systems, 2026, first author
- **Within-Camera Multilayer Perceptron DVS Denoising**, CVPR Workshop, 2023

SKILLS

Languages	SystemVerilog (RTL, DV, SVA), Python, C/C++, Bash, Tcl, OpenCL
Security/DV	Formal Verification, UVM, SVA, Hardware Fuzzing
EDA Tools	AMD/Xilinx Vivado & Vitis, Cadence Genus & Innovus, Synopsys Design Compiler
Verification Tools	Verilator, Synopsys VCS, AMD Xsim, Questa Formal, SymbiYosys, Cocotb
Other	Git, Docker, LaTeX, GitHub Actions, QKeras, PyTorch